Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A computer implemented method of simulating a logic design, the method comprising:

storing a first state to identify in a simulation of a logic design whether a node included in the logic design has a logic high value;

storing a second state to identify in simulation of the logic design whether the node has a logic low value;

storing a third state to identify in simulation of the logic design whether the node has an undefined state; and

performing a three state simulation of the logic design to determine an output of the node in simulation of the logic design based on the first state, the second state, and the third state; and

determining if the three state simulation of the logic design was successful, based on whether the output of the node has an undefined state, the three state simulation being successful if the output of the node is a defined state; and

performing a four state simulation of the logic design if the three state simulation of the logic design was successful.

2. (Previously Presented) The computer implemented method of claim 1 further comprising determining whether the output of the node in simulation of the logic design has a high impedance state based on the first state, the second state, and the third state.

3. (Previously Presented) The computer implemented method of claim 1 further comprising storing the third state only if at least two sources drive the node.

4. (Canceled)

5. (Previously Presented) The computer implemented method of claim 1 further comprising:

determining the output based on which of the first state, the second state, and the third state is at a logic high.

6. (Previously Presented) An article for simulating a logic design, the article comprising:

a machine readable medium which contains machine executable instructions, the instructions causing a machine to:

store a first state to identify in a simulation of a logic design whether a first node included in the logic design has a logic high value;

store a second state to identify in simulation of the logic design whether the first node has a logic low value;

store a third state to identify in simulation of the logic design whether the first node has an undefined state; and

perform a three state simulation of the logic design to determine an output of the node in simulation of the logic design based on the first state, the second state, and the third state; and

determine if the three state simulation of the logic design was successful, based on whether the output of the node has an undefined state, the three state simulation being successful if the output of the node is a defined state; and

perform a four state simulation of the logic design if the three state simulation of the logic design was successful.

7. (Original) The article of claim 6 further causing a machine to determine whether the output of the node in simulation of the logic design has a high impedance state based on the first state, the second state, and the third state.

8. (Original) The article of claim 6 further causing a machine to store the third state only if at least two sources drive the node.

9. (Canceled)

10. (Original) The article of claim 6 further causing a machine to:

determine the output based on which of the first state, the second state, and the third state is at a logic high.

11. (Previously Presented) An apparatus for simulating a logic design, the apparatus comprising:

a memory that stores executable instructions; and

a processor that executes the instructions to:

store a first state to identify in a simulation of a logic design whether a first node included in the logic design has a logic high value,

store a second state to identify in simulation of the logic design whether the first node has a logic low value,

store a third state to identify in simulation of the logic design whether the first node has an undefined state, and

perform a three state simulation of the logic design to determine an output of the node in simulation of the logic design based on the first state, the second state, and the third state; and

determine if the three state simulation of the logic design was successful, based on whether the output of the node has an undefined state, the three state simulation being successful if the output of the node is a defined state; and

perform a four state simulation of the logic design if the three state simulation of the logic design was successful.

12. (Original) The apparatus of claim 11 further executing the instructions to determine whether the output of the node in simulation of the logic design has a high impedance state based on the first state, the second state, and the third state.

13. (Original) The apparatus of claim 11 further executing the instructions to store the third state only if at least two sources drive the node.

14. (Original) The apparatus of claim 11 further executing the instructions to perform four state simulation of the logic design subsequent to the simulation of the logic design if the simulation of the logic design was successful.

15. (Original) The apparatus of claim 11 further executing the instructions to determine the output based on which of the first state, the second state, and the third state is at a logic high.

16-24. (Canceled)